R22 Regulation *Subject code:4E3DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, June 2026

DIGITAL LOGIC DESIGN

(ECE)

Maximum Marks: 60 Date:11.06.2026 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X1M=10 Marks)		Marks	CO	BTL
1.a)	Add (+70) and (-60) using 2's complement	1M	1	L2
b)	Convert $(67A9)_{16}$ into decimal.	1M	1	L2
c)	What are minterms? Give any two examples.	1M	2	L2
d)	What are universal gates?	1M	2	L2
e)	Write the full subtractor truth table.	1M	3	L2
f)	Give the function of a multiplexer.	1M	3	L2
g)	Write down the characteristic equation of S-R flipflop.	1M	4	L2
h)	Draw the logic diagram of a master slave J-K flip-flop.	1M	4	L2
i)	Draw the circuit diagram of Ring counter.	1M	5	L2
j)	What is counter?	1M	5	L2

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
2	Perform the subtraction with the following binary numbers using 2's complement. (a)11010 - 1101 (b) 11010 -10000 (c) 10010 - 10011 (d) 100 - 110000	10M	1	L3
	OR			
3	a) Represent $(524)_{10}$ in 2421 code and Excess-3 code. b) Simplify $x + xyz + yzx' + wx + w'x + xy$ using Boolean algebra. .	5M 5M	1	L3
4	Find the Simplified expression using K-map and design with NAND gates F (A, B, C, D) =$\sum$ m (0,1,2,9,11) + d (8,10,14,15)	10M	2	L3
	OR			
5	a) Simplify the following equation by K-Map F(A, B, C) = $\sum$m(0, 2, 4) + $\sum$d(1, 3, 5, 6, 7). b) Implement the function F = x' y + x y' + z using NOR gates only.	5M 5M	2	L3
6	Explain the construction, working principle of a half adder and a full adder and draw its block diagram?	10M	3	L2

	OR			
7	Explain the Design of a 3-bit magnitude comparator. Analyze its performance.	10M	3	L2
8	Explain the operation of clocked SR flip-flop with its characteristic table and Excitation table.	10M	4	L2
	OR			
9	Draw the logic diagram of a JK flip flop and explain its operation with relevant truth tables.	10M	4	L3
10	a) What is a hazard? How do you eliminate hazards? b) Design and explain Johnson counter.	5M 5M	5	L2
	OR			
11	Draw the circuit diagram of a 4-bit binary counter with parallel load and explain its working with its function table.	10M	5	L3